This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Currently Amended) [The device of claim 2, further comprising] A device to determine a resistive load connected to a source of alternating current ("AC") power, comprising:

a. a signal path and an AC power path, both paths connected to a device input and a device output;

b. a processor connected to a sensing circuit including a sensing resistor that determines a current level in said AC power path, said processor indicating an off condition according to said current level on said sensing resistor;

c. a control circuit that turns off said AC power to said device output when instructed by said processor at said off condition, wherein said control circuit comprises a first field effect transistor and a second field effect transistor coupled to a transistor, said transistor coupled to the gates of said first and second field effect transistors; and

d. a circuit to control AC power to a load, comprising:

a1. a first resistor and an electronic switch connected in series to a source of direct current ("DC") power;

b1. said first field effect transistor having a drain connected in series with said load and said AC power;

c1. said second field effect transistor having a source connected in series with a source of said first field effect transistor, wherein the drain of said second field effect transistor is connected to ground;

d1. a clamping diode having a cathode and an anode, wherein said cathode is connected to the [source] gate of each of said first and second field effect transistors, and wherein the anode of said clamping diode is connected to [a gate] the source of each of said first and second field effect transistors and to the end of said series connection of said electronic switch and said first resistor opposite to said DC power source; and

e1. a second resistor connected in parallel to said clamping diode.

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Currently Amended) A circuit to control alternating current ([A]AC[@]) power to a load, comprising:

a. a first resistor and an electronic switch connected in series to a source of direct current ("DC") power;

b. a first FET transistor having a drain connected in series with said load and said AC power;

c. a second FET transistor having a source connected in series with a source of said first FET transistor, wherein the drain of said second FET transistor is connected to ground;

d. a clamping diode having a cathode and an anode, wherein said cathode is connected to the [source] gate of each of said first and second FET transistors, and wherein the anode of said clamping diode is connected to [a gate] the source of each of said first and second FET transistors and to the end of said series connection of said switch and said first resistor opposite to said DC power source; and

e. a second resistor connected in parallel to said clamping diode.

20. (Original) The circuit of claim 19, wherein said clamping diode is a Zener diode having a breakdown voltage rating lower than the gate-to-source breakdown voltage of the said first and second FETS.

21. (Original) The circuit of claim 19, wherein said switch comprises a transistor.

22. (Original) The circuit of claim 21, wherein said transistor is a PNP transistor having an emitter connected to the DC power source and a collector connected to the first lead of said first resistor.

23. (Cancelled)

24. (Cancelled)

25. (Original) A circuit to sense positive and negative over-voltage, comprising:

a. a first transistor connected to a sense resistor having a current;

b. a second transistor connected to said sense resistor; and

c. a first voltage reference connected to said first transistor and a second voltage reference connected to said second transistor, said voltage references providing a sense setting to said first and second transistors, wherein said first transistor is configured to have an on condition when said input voltage is above a first predetermined level as sensed by said current in said sense resistor, and said second transistor having an on condition when said input voltage is below a second predetermined level as sensed by said current in said sense resistor.

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)